

STATUS OF THE CLAIMS

The status of the claims of the present application stands as follows:

Claim 1-17: (Canceled)

18. (Previously presented) A device according to claim 19, further comprising a first hardmask remnant located substantially only between said second spacer and said upper surface of said source and a second hardmask remnant located between said third spacer and said upper surface of said drain portion.

19. (Currently amended) A device, comprising:

an integrated circuit formed on a substrate and comprising a plurality of FETs wherein at least some of said plurality of FETs are finFETs each comprising:

- a) a fin having a source portion, a drain portion and a channel portion extending between said source portion and said drain portion, said fin having a base portion disposed on said substrate, each of said source portion and said drain portion having an upper surface, said fin having a length extending from, and including, said source portion and said drain portion, and each of said source portion and said drain portion including an upper surface having a width;
- b) a first spacer formed adjacent said base portion;
- c) a gate located at said channel portion;
- d) a first reentrant corner between said upper surface of said source portion and said gate;
- e) a second reentrant corner between said upper surface of said drain portion and said gate;
- f) a second spacer proximate said first reentrant corner and having a length extending along said gate substantially equal to said width of said source portion immediately adjacent said gate; and
- g) a third spacer proximate said second reentrant corner and having a length extending along said gate substantially equal to said width of said drain portion immediately adjacent said gate.

20. (Previously presented) A device according to claim 19, wherein said first spacer comprises silicon dioxide.

21. (Previously presented) A device according to claim 19, wherein said substrate comprises an undercut region beneath at least a portion of said fin, said undercut region containing at least a portion of said first spacer.

22. (Currently amended) An integrated circuit, comprising:

- a) a substrate; and
- b) a plurality of FETs formed on said substrate, wherein at least some of said plurality of FETs are finFETs each comprising:
 - i) a fin that includes a source having a base disposed on said substrate and further includes a drain and a channel extending between said source and said drain, said fin having a length extending from, and including, said source and said drain portion, and each of said source portion and said drain including an upper surface having a width; and
 - ii) a first spacer formed at least adjacent the entire said base portion of said source;
- c) a gate located at said channel;
- d) a first reentrant corner between said upper surface of said source and said gate;
- e) a second reentrant corner between said upper surface of said drain and said gate;
- f) a second spacer proximate said first reentrant corner and having a length extending along said gate substantially equal to said width of said source immediately adjacent said gate; and
- g) a third spacer proximate said second reentrant corner and having a length extending along said gate substantially equal to said width of said drain immediately adjacent said gate.

23. (Canceled)

24. (Currently amended) An integrated circuit according to claim 22, further comprising a first hardmask remnant located between said second spacer and said upper surface of said source and a second hardmask remnant located between said third spacer and said upper surface of said drain.

25. (Previously presented) An integrated circuit according to claim 22, wherein said first spacer comprises silicon dioxide.

26. (Previously presented) An integrated circuit according to claim 22, wherein said substrate comprises an undercut region beneath at least a portion of said fin, said undercut region containing at least a portion of said first spacer.

27. (Previously presented) A finFET formed on a substrate, comprising:

- a) a fin having a source, a drain and a channel extending between said source and said drain, said fin having a length extending from, and including, said source and said drain, and each of said source and said drain including an upper surface having a width;
- b) a gate located at said channel;
- c) a first reentrant corner between said upper surface of said source and said gate;
- d) a second reentrant corner between said upper surface of said drain and said gate;
- e) a first spacer proximate said first reentrant corner and having a length extending along said gate substantially equal to said width of said source immediately adjacent said gate; and
- f) a second spacer proximate said second reentrant corner and having a length extending along said gate substantially equal to said width of said drain immediately adjacent said gate.

28. (Previously presented) A finFET according to claim 27, wherein each of said source and said drain includes a base attached to the substrate, the finFET further comprising a third spacer formed adjacent the base of said source.

29. (Previously presented) A finFET according to claim 27, further comprising a first hardmask remnant located substantially only between said first spacer and said upper surface of said source and a second hardmask remnant located substantially only between said second spacer and said upper surface of said drain.

30. (Previously presented) A finFET according to claim 27, wherein said first spacer comprises silicon dioxide.

31. (Previously presented) A finFET according to claim 27, wherein the substrate comprises an undercut region beneath at least said base of said source, the undercut region containing at least a portion of said first spacer portion.

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